C.U.SHAH UNIVERSITY Summer Examination-2017

Subject Name: Analog VLSI Design Subject Code: 5TE02AVD1

Branch: M.Tech (VESD)

Semester: 2	Date: 04/05/2017	Time: 02:00 To 05:00	Marks: 70

Instructions:

- (1) Use of Programmable calculator and any other electronic instrument is prohibited.
- (2) Instructions written on main answer book are strictly to be obeyed.
- (3) Draw neat diagrams and figures (if necessary) at right places.
- (4) Assume suitable data if needed.

SECTION – I

Q-1		Define the following terms	(07)
	a.	Threshold voltage	
	b.	Cascode current source	
	c.	Common mode rejection ratio.	
	d.	Short channel	
	e.	Slew Rate	
	f.	Subthreshold current	
	g.	Current Mirror.	
Q-2		Attempt all questions	(14)
·	(a)	Explain in detail developing of the Beta-multiplier reference.	
	(b)	Explain Low-Voltage (Wide-Swing) Cascode in detail.	
		OR	
Q-2		Attempt all questions	(14)
	(a)	Explain in detail the DC operation of Source-Coupled Pair.	
	(b)	Explain Biasing of the Cascode Current Source and its operation.	
Q-3		Attempt all questions	(14)
	(a)	Explain Threshold Voltage Mismatch Current Mirror circuit.	
	(b)	Explain Diff-amp with a current mirror load.	
	<u> </u>	OR	
Q-3		Attempt all questions	(14)
	(a)	Explain Transconductance Parameter Mismatch Current Mirror circuit.	

Explain the current mirror and its equivalent circuit representation of a current **(b)** source.





Q-4		Define the following terms	(07)
C	a.	Comparator.	
	b.	Clock Skew.	
	c.	Phase Noise.	
	d.	Timing Jitter.	
	e.	Charge pump.	
	f.	VCO.	
	g.	Adaptive Biasing.	
Q-5		Attempt all questions	(14)
τ	(a)	Explain in detail basic Clocked Comparators.	()
	(b)	Explain the Positive feedback decision circuit in detail.	
		OR	
Q-5		Attempt all questions	(14)
τ-	(a)	Draw and explain the Preamplification stage of comparator.	()
	(b)	Explain the CMOS implementation of the Astable multivibrator.	
Q-6		Attempt all questions	(14)
· ·	(a)	Explain the basic schematic of the Schmitt trigger using CMOS.	
	(b)	Explain the Phase Frequency Detector in detail.	
		OR	
Q-6		Attempt all Questions	(14)
τv	(a)	Draw and explain Delay Locked Loop in detail.	()
	(b)	Draw and explain the CMOS peak detector.	
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